REMARKS

The Office Action mailed January 2, 2003, has been received and reviewed. Claims 1, 4 through 10, and 13 through 20 are currently pending in the application. Claims 1, 4 through 10, and 13 through 20 stand rejected. Reconsideration is respectfully requested.

Claim Objections

Claim 9 stands objected to because it depends from a canceled claim. Claim 9 has been amended to depend from pending claim 1.

35 U.S.C. § 112 Claim Rejections

Claims 1, 4 through 10, and 13 through 20 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Specifically, it was stated that the phrase "a substantially dopant-free TEOS" layer was not described in the specification. Applicants respectfully submit that this claim element is inherently disclosed in the specification. However, in an effort to expedite prosecution, applicants have removed this element from claims 1 and 10. Reconsideration and withdrawal of the rejection is requested.

Claims 9 and 20 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Specifically, it was stated that it was not clear whether the TEOS layer included a second dopant barrier or whether the TEOS layer was the dopant barrier. Applicants respectfully submit the claims are not indefinite. However, applicants have amended claims 9 and 20 to recite the

"TEOS layer is a dopant barrier". Further, applicants have replaced the phrase "insulating layer" with "BPSG layer". Reconsideration and withdrawal of the rejection is requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent 6,274,423 to Prall et al. in View of U.S. Patent 6,124,626 to Sandhu et al.

Claims 1, 4, 6 through 10, 13 through 15, 17 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al.(U.S. Patent 6,274,423) previously applied, in view of Sandhu et al. (U.S. Patent 6,124,626) previously applied. Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Prall discloses an etch process for aligning a capacitor and an adjacent contact corridor. Sandu discloses capacitor structures formed using excess oxygen containing materials.

By way of contrast with the combined references, claim 1 of the presently claimed invention recites a "DRAM circuit comprising: a substrate having a capacitor structure disposed thereon, said capacitor structure including a storage node, a dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate; a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between

said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer."

Applicants respectfully submit that the combined references fail to teach or suggest every element of the presently claimed invention. Specifically, neither Prall nor Sandhu teach or suggest "a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer."

Instead, Prall lacks fails to teach or suggest a TEOS layer, a BPSG layer disposed over said TEOS layer or a conductive contact extending through a doped BPSG layer and TEOS layer. Similarly, Sandhu lacks disclosure of a doped BPSG layer disposed over a TEOS layer, end portions or any conductive contact. Applicants respectfully submit that Sandu fails to teach or suggest that region 53 is a BPSG layer. (Sandhu, col. 6, lines 54-56). As the proposed combination of references fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 1 is not rendered obvious by the cited references. Thus, claim 1 is allowable.

Further, applicants respectfully submit that no motivation exists in the cited references for their combination. Prall is directed toward an etch process for aligning a capacitor structure and adjacent contact corridor. Sandhu discloses that the ozone enhanced TEOS layer protects against oxygen leaks. Sandhu lacks any disclosure that a TEOS layer would provide any benefit to the capacitor structure in Prall. Further, as Sandhu fails to teach or suggest end portions proximate a conductive contact, no motivation exists to form a TEOS layer that encases end portions of the dielectric layer and conductive cell plate in Prall. As no motivation exists to combine the references, applicants submit that independent claim 1 of the presently claimed invention is not rendered obvious. Thus, claim 1 is allowable.

Claims 4 through 9 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 9 is further allowable as neither Prall nor Sandhu teaches or suggest that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

Claim 10 of the presently claimed invention is allowable at least for the same reasons as claim 1. Claim 10 of the presently claimed invention recites a "semiconductor memory device comprising: a semiconductor substrate having a capacitor structure formed thereon, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer; a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer".

Applicants respectfully submit that the combined references fail to teach or suggest every element of the presently claimed invention. Specifically, neither Prall nor Sandhu teach or suggest "a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer."

Instead, Prall lacks fails to teach or suggest a TEOS layer, a BPSG layer disposed over said TEOS layer or a conductive contact extending through a doped BPSG layer and TEOS layer. Similarly, Sandhu lacks disclosure of a doped BPSG layer disposed over a TEOS layer, end portions or any conductive contact. Applicants respectfully submit that Sandu fails to teach or suggest that region 53 is a BPSG layer. As the proposed combination of references fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 10 is not rendered obvious by the cited references. Thus, claim 10 is allowable.

Further, applicants respectfully submit that no motivation exists in the cited references for their combination. Prall is directed toward an etch process for aligning a capacitor structure and adjacent contact corridor. Sandhu discloses that the ozone enhanced TEOS layer protects against oxygen leaks. Sandhu lacks any disclosure that a TEOS layer would provide any benefit to the capacitor structure in Prall. Further, as Sandhu fails to teach or suggest end portions proximate a conductive contact, no motivation exists to form a TEOS layer that encases end portions of the dielectric layer and conductive cell plate in Prall. As no motivation exists to combine the references, applicants submit that independent claim 10 of the presently claimed invention is not rendered obvious. Thus, claim 10 is allowable.

Claims 13 through 20 are each allowable as depending, either directly or indirectly, from allowable claim 10.

Claim 20 is further allowable as neither Prall nor Sandhu teaches or suggest that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

Obviousness Rejection Based on U.S. Patent 6,274,423 to Prall et al. and U.S. Patent 6,124,626 to Sandhu et al. and Further in View of U.S. Patent 5,763,306 to Tsai

Claims 5 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al.(U.S. Patent 6,274,423) previously applied, and Sandhu et al. (U.S. Patent 6,124,626) previously applied, as applied to claims 1 through 4, 6 through 9, 10 through 15, and 17 through 20 above, and further in view of Tsai (U.S. Patent 5,763,306) previously applied. Applicants respectfully traverse this rejection, as hereinafter set forth.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 5 and 16 obvious, cannot serve as a basis for rejection.

ENTRY OF AMENDMENTS

The amendments to the claims above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1, 4 through 10, and 13 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should additional issues remain which might be resolved by a telephone conference, the Office is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Krista Weber Powell
Registration No. 47,867
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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JAW/ps:ljb

Enclosure: Version With Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended twice) A DRAM circuit comprising:

a substrate having a capacitor structure disposed thereon, said capacitor structure including a storage node, a dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion[;] proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate;

a [substantially dopant-free] TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer.

9. (Amended twice) The DRAM circuit of claim [2] 1, wherein said TEOS layer is [comprises] a dopant barrier between said capacitor structure and said [insulating] BPSG layer.

10. (Twice Amended) A semiconductor memory device comprising:

a semiconductor substrate having a capacitor structure formed thereon, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion[;] proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer;

a [substantially dopant-free] TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact; and

a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer.

20. (Amended three times) The device of claim 10, wherein said TEOS layer [comprises] is a dopant barrier between said capacitor structure and said [insulating] BPSG layer.